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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/757,373
Filing Date	January 14, 2004
First Named Inventor	Kazumi HARA
Art Unit	2826
Examiner Name	Alexander O. Williams
Total Number of Pages in This Submission	Attorney Docket Number: 9319I-000647

ENCLOSURES ***(check all that apply)***

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) ____
- ☐ After Allowance Communication to Technology Center (TC)
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below)*:
  Acknowledgement Postcard

Remarks

The Commissioner is hereby authorized to charge any additional fees that may be required under 37 CFR 1.16 or 1.17 to Deposit Account No. 50-3213 (Epson R & D). A duplicate copy of this sheet is enclosed.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Harness, Dickey & Pierce, P.L.C.	Attorney Name G. Gregory Schivley Bryant E. Wade	Reg. No. 27,382 40,344
Signature			
Date	November 30, 2006		

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	G. Gregory Schivley Bryant E. Wade	Express Mail Label No.	EV 757 778 445 US
Signature		Date	November 30, 2006

EV 757 778 445 US

HDP/SB/17 (02-06)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2006

Effective 2/8/2006. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500

Complete if Known	
Application Number	10/757,373
Filing Date	January 14, 2004
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Art Unit	2826
Attorney Docket No.	9319I-000647

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: 50-3213

Deposit Account Name: Epson R & D

The Director is authorized to: *(check all that apply)*
☒ Charge fee(s) indicated below ☒ Credit any overpayments
☒ Charge any additional fee(s) during the pendency of this application
☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1011	300	2011	150	Utility filing fee	
1012	200	2012	100	Design filing fee	
1013	200	2013	100	Plant filing fee	
1014	300	2014	150	Reissue filing fee	
1005	200	2005	100	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20 **	= 0	X		=	0
Independent Claims		-3 **	= 0	X		=	0
Multiple Dependent						=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple dependent claim, if not paid
1204	200	2204	100	** Reissue independent claims over original patent
1205	50	2205	25	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500
1403	1000	2403	500	Request for oral hearing	
1452	500	2452	250	Petition to revive – unavoidable	
1453	1500	2453	750	Petition to revive – unintentional	
1462	400	1462	400	Petition fee under 37 CFR 1.17(f)	
1463	200	1463	200	Petition fee under 37 CFR 1.17(g)	
1464	130	1464	130	Petition fee under 37 CFR 1.17(h)	
1807	50	1807	50	Processing fee under 37 CFR 1.17 (q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
				Other fee (specify) ____	

***Reduced by Basic Filing Fee Paid** SUBTOTAL (3) ($)500

4. SEARCH/EXAMINATION FEES

1111	500	2111	250	Utility Search Fee	
1112	100	2112	50	Design Search Fee	
1113	300	2113	150	Plant Search Fee	
1114	500	2114	250	Reissue Search Fee	
1311	200	2311	100	Utility Examination Fee	
1312	130	2312	65	Design Examination Fee	
1313	160	2313	80	Plant Examination Fee	
1314	600	2314	300	Reissue Examination Fee	

SUBTOTAL (4) ($)0

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	G. Gregory Schivley Bryant E. Wade	*Registration No. (Attorney/Agent)*	27,382 40,344	*Telephone*	(248) 641-1600
Signature				*Date*	November 30, 2006

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/757,373
Filing Date:	January 14, 2004
Applicant:	HARA, Kazumi
Group Art Unit:	2826
Examiner:	Alexander O. Williams
Title:	SEMICONDUCTOR CHIP AND SEMICONDUCTOR WAFER INCLUDING A VARIABLE THICKNESS INSULATING LAYER
Attorney Docket:	9319I-000647

Director of the U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Attention: Board of Patent Appeals and Interferences

APPELLANT'S BRIEF (37 C.F.R. 41.37)

This brief is in furtherance of the Notice of Appeal filed on October 24, 2006. The fee required under 37 C.F.R. 41.20(b)(2) is authorized for payment from Applicant's deposit account in the accompanying transmittal form.

TABLE OF CONTENTS

This brief contains these items under the following headings, and in the order set forth below:

The final page of this brief bears the practitioner's signature.

I. REAL PARTY IN INTEREST

The real party in interest is Seiko Epson Corporation, the assignee of record.

II. RELATED APPEALS AND INTERFERENCES

There are no other prior or pending appeals, judicial proceedings, or interferences known to Applicant which may be related to, directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

The status of the claims in this application is:

a. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are 1 – 70.

b. STATUS OF ALL THE CLAIMS

i. Claims cancelled: 1-4, 9-18, 23-33, 35-41 and 43-70

ii. Claims allowed: none

iii. Claims rejected: 5-8, 19-22, 34 and 42

iv. Claims withdrawn: none

v. Claims objected to: none

c. CLAIMS ON APPEAL

The claims on appeal are 5-8, 19-22, 34 and 42.

IV. STATUS OF AMENDMENTS

The final office action was mailed July 25, 2006. Applicant responded September 22, 2006 without amending the claims. An advisory action was mailed October 6, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

As called for in independent claim 5 and illustrated in Figs. 1A – 4 and 13, a semiconductor chip 80 is provided. The chip comprises a semiconductor substrate 10 (page 19, lines 4-5), an integrated circuit 12 (page 19, lines 5-7), a penetrating electrode 40 (page 23, lines 16-17), and an insulating layer 50 (page 23, line 19). At least a part of the integrated circuit 12 is formed in the semiconductor substrate 10 (page 19, lines 3-9). The penetrating electrode 40 is formed in a through-hole 22 (introduced as recess 22 at page 19, lines 24-25 and then illustrated as a complete through-hole at least at Fig. 4) of the semiconductor substrate 10 from a first surface 20 to a second surface 38 of the semiconductor substrate 10 (page 23, lines 15-18). The through-hole 22 has sidewalls entirely orthogonal to the first surface 20 and the second surface 38 (see e.g., Fig. 4). The penetrating electrode 40 has a projection 42 which projects from the second surface 38 (page 23, lines 16-17). The insulating layer 50 is formed over an entire surface of the second surface 38 of the substrate 10 (page 23, lines 19-21). The insulating layer 50 includes a first insulating section 52 formed in a region that surrounds the projection 42 (page 23, lines 23-24) such that the projection 42 forms a through-bore in the first insulating section 52 above the second surface 38 of the

substrate 10 (see e.g., Fig. 4). The second insulating section 54 covers a remaining region of the second surface 38 of the semiconductor substrate 10 (page 24, lines 6-10 and Fig. 4). The first insulating section 52 is connected to the second insulating section 54 by a radially tapering arcuate portion having a varying radius of curvature from the through-bore to the second insulating section 54 (page 24, lines 1-2, and e.g., Fig. 4). The second insulating section 54 is formed to be thinner than a thickest area of the first insulating section 52 (page 24, lines 7-10).

As called for in dependent claim 6, the first insulating section 52 may be formed so that a thickness of the first insulating section 52 decreases as a distance from the projection 42 increases (page 24, lines 1-2).

As called for in dependent claim 7, the projection 42 may be formed to have a height higher than a height of a thickest area of the insulating layer 50 (page 25, lines 3-5).

As called for in dependent claim 8, the projection 42 may be formed to have a height equal to a height of a thickest area of the insulating layer 160 (page 26, lines 8-10).

As called for in independent claim 19 and illustrated in Figs. 1A -4 and 11 - 13, a semiconductor wafer 70 is provided. The wafer comprises a semiconductor substrate 10, a plurality of integrated circuits 12, a plurality of penetrating electrodes 40, and an insulating layer 50 (page 29, lines 16-25 and as described above with respect to claim 5). At least a part of each of the integrated circuits 12 is formed in the semiconductor substrate 10 (page 19, lines 3-9). Each of the plurality of penetrating electrodes 40 is formed in through-holes 22 (page 19, lines 24-25 and Fig. 4) of the semiconductor

substrate 10 from a first surface 20 to a second surface 38 of the semiconductor substrate 10 (page 23, lines 15-18). The through-holes 22 have sidewalls entirely orthogonal to the first surface 20 and the second surface 38 (see e.g., Fig. 4). Each of the penetrating electrodes 40 have a projection 42 which projects from the second surface 38 (page 23, lines 16-17). The insulating layer 50 is formed over an entire surface of the second surface 38 of the substrate 10 (page 23, lines 19-21). The insulating layer 50 includes a plurality of first insulating sections 52 and a second insulating section 54 other than the first insulating sections 52. Each of the first insulating sections 52 is formed in regions that surround the projections 42 (page 23, lines 23-24) above the second surface 38 of the substrate 10 such that the projections 42 define through-bores in the first insulating sections 52 (see e.g., Fig. 4). The second insulating section 54 covers a remaining region of the second surface 38 of the semiconductor substrate 10 (page 24, lines 6-10). The first insulating sections 52 are connected to the second insulating section 54 by radially tapering arcuate portions having a varying radius of curvature from the through-bore to the second insulating section 54 (page 24, lines1-2, and e.g., Fig. 4). The second insulating section 54 is formed to be thinner than a thickest area of each of the first insulating sections 52 (page 24, lines 7-10).

As called for in dependent claim 20, each of the first insulating sections 52 may be formed so that a thickness of each of the first insulating sections 52 decreases as a distance from the projection 42 increases (page 24, lines 1-2).

As called for in dependent claim 21, the projection 42 may be formed to have a height higher than a height of a thickest area of the insulating layer (page 25, lines 3-5).

As called for in dependent claim 22, the projection 42 may be formed to have a height equal to a height of a thickest area of the insulating layer 160 (page 26, lines 8-10).

As called for in claim 34, a circuit board 1000 is provided on which the semiconductor chip 10 as defined in claim 5 is mounted (page 32, lines 13-15).

As called for in dependent claim 42, an electronic instrument 2000 or 3000 is provided that comprises the semiconductor chip 10 as defined in claim 5 (page 32, lines 15-17).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

a. Whether claims 5-8, 34 and 42 are unpatentable under 35 U.S.C. 103 over Siniaguine.

b. Whether claims 19-22 are unpatentable under 35 U.S.C. 103 over Siniaguine in view of Patti.

VII. ARGUMENTS

a. Rejection under 35 U.S.C. 103 over Siniaguine

i. Claims 5-8, 34 and 42

According to MPEP 2143.03 and the cases cited therein, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art.

Claim 5 recites that an insulating layer is formed over an entire surface of a second surface of a substrate. This is shown, for example, in Figure 4 where the

insulating layer 50 is formed over an entire surface of the second surface 38 of the substrate 10. The Final Office Action alleges that Siniaguine teaches an insulating layer 140 that is formed over an entire surface of a second surface of a substrate 110.

Upon review of Siniaguine, however, no such teaching exists. At best, Siniaguine merely teaches an insulating layer 140 that terminates on a surface of the protruding electrode 160. The alleged insulating layer 140, however, is not disposed over any portion of the second surface of the substrate 110, as claimed. Because the alleged insulting layer 140 of Siniaguine does not cover an entire surface of the second surface of the substrate, as claimed, Applicant respectfully asserts that independent Claim 5 and dependent claims 6-8, 34 and 42 are not obvious in view of Siniaguine.

b. Rejection under 35 U.S.C. 103 over Siniaguine in view of Patti

i. Claims 19-22

As stated above, according to MPEP 2143.03 and the cases cited therein, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art.

Claim 19 recites that an insulating layer is formed over an entire surface of a second surface of a substrate. As stated above, Siniaguine fails to teach an insulating layer formed over an entire surface of the claimed second surface of the substrate. Since Siniaguine is silent with respect to this aspect of the claimed invention, Siniaguine cannot render independent Claim 19 nor dependent claims 20-22 obvious even if combined with the teachings of Patti.

c. Advisory Action

As argued above, the final office action alleges that element 140 of Siniaguine corresponds to the claimed insulating layer in the present application. In the response after final, Applicant argued that element 140 of Siniaguine does not cover an entire surface of the second surface of the substrate, as claimed. The advisory action mailed October 6, 2006 states that Siniaguine figure 10 shows that the insulating layer 1010 is formed over the entire surface of the second surface of the substrate. Supposing that element 1010 corresponds to the claimed insulating layer claimed, Siniaguine still cannot render the claimed invention obvious.

More particularly, independent claims 5 and 19 call for an insulating layer (50) having a first insulating section (52) and a second insulating section (54). The first insulating section (52) is connected to the second insulating section (54) by a radially tapering arcuate portion having a varying radius of curvature from a through-bore to the second insulating section (54). See for example, Fig. 4. Element 1010 in Siniaguine does not include this feature. Therefore, Siniaguine cannot render the claims obvious even if combined with Patti.

VIII. CLAIMS APPENDIX

The text of the claims involved in the appeal is:

5. A semiconductor chip comprising:

a semiconductor substrate;

an integrated circuit, at least a part of the integrated circuit being formed in the semiconductor substrate;

a penetrating electrode which is formed in a through-hole of the semiconductor substrate from a first surface to a second surface of the semiconductor substrate, the through-hole having sidewalls entirely orthogonal to the first and second surface, and the penetrating electrode having a projection which projects from the second surface; and

an insulating layer formed over an entire surface of the second surface of the substrate, the insulating layer including a first insulating section formed in a region that surrounds the projection such that the projection forms a through-bore in the first insulating section above the second surface of the substrate, and a second insulating section that covers a remaining region of the second surface of the semiconductor substrate, the first insulating section being connected to the second insulating section by a radially tapering arcuate portion having a varying radius of curvature from the through-bore to the second insulating section;

wherein the second insulating section is formed to be thinner than a thickest area of the first insulating section.

6. The semiconductor chip as defined in claim 5, wherein the first insulating section is formed so that a thickness of the first insulating section decreases as a distance from the projection increases.

7. The semiconductor chip as defined in claim 5, wherein the projection is formed to have a height higher than a height of a thickest area of the insulating layer.

8. The semiconductor chip as defined in claim 5, wherein the projection is formed to have a height equal to a height of a thickest area of the insulating layer.

19. A semiconductor wafer comprising:

a semiconductor substrate;

a plurality of integrated circuits, at least a part of each of the integrated circuits being formed in the semiconductor substrate;

a plurality of penetrating electrodes, each of the penetrating electrodes being formed in through-holes of the semiconductor substrate from a first surface to a second surface of the semiconductor substrate, the through-holes having sidewalls entirely orthogonal to the first and second surface, and the penetrating electrodes each having a projection which projects from the second surface; and

an insulating layer formed over an entire surface of the second surface of the substrate, the insulating layer including a plurality of first insulating sections and a second insulating section other than the first insulating sections, each of the first insulating sections being formed in regions that surround the projections above the

second surface of the substrate such that the projections define through-bores in the first insulating sections, and the second insulating section covering a remaining region of the second surface of the semiconductor substrate, the first insulating sections being connected to the second insulating section by radially tapering arcuate portions having a varying radius of curvature from the through-bore to the second insulating section;

wherein the second insulating section is formed to be thinner than a thickest area of each of the first insulating sections.

20. The semiconductor wafer as defined in claim 19, wherein each of the first insulating sections is formed so that a thickness of each of the first insulating sections decreases as a distance from the projection increases.

21. The semiconductor wafer as defined in claim 19, wherein the projection is formed to have a height higher than a height of a thickest area of the insulating layer.

22. The semiconductor wafer as defined in claim 19, wherein the projection is formed to have a height equal to a height of a thickest area of the insulating layer.

34. A circuit board on which the semiconductor chip as defined in claim 5 is mounted.

42. An electronic instrument comprising the semiconductor chip as defined in claim 5.

IX. EVIDENCE APPENDIX

None

X. RELATED PROCEEDINGS APPENDIX

None

Respectfully submitted,

Dated: Nov 30, 2006

By: _____
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